What is claimed is:

1. A method for an image reducing processing circuit including the memory architecture of two First-In-First-Out (FIFO) units for simplifying the using of access frequency and memory depth, said method comprising the following steps of:

(1) providing an input processing receiving input image data and delivering said image data;

(2) providing a horizontal direction image processing receiving said image data from said step(1), quantifying said image data in said horizontal direction, and then transferring said image data to column signals with a row column type ;

(3) providing a first step First-In-First-Out (FIFO) receiving said image data from said step(2) to read and write said image data with said first access frequency, and having a plurality of First-In-First-Out (FIFO) sub unit receiving and delivering said image data in sequence;

(4) providing a vertical direction image processing receiving said image data from said step(3), reading and writing completely said image data, quantifying said image data in said vertical direction, and then transferring said image data to row signals with a row column type;

(5) providing a second step First-In-First-Out (FIFO) receiving said image data from said step(4), and having a First-In-First-Out (FIFO) memory element implementing said readout and writing of said image data on said first access

frequency and a second access frequency; and

(6) providing an output processing working on the second access frequency, receiving said image data from said setp(5), and outputting reduced image data.

2. The method for an image reducing processing circuit according to claim 1, wherein said input image data received by said input processing unit are original image data.

3. The method for an image reducing processing circuit according to claim 1, wherein said output processing unit is a medium means for outputting image data.

4. The method for an image reducing processing circuit according to claim 1, wherein providing a first step First-In-First-Out (FIFO) unit receiving said image data and delivering said image data in sequence includes the following steps:

(1) reading said image data in said horizontal direction, and writing said image data into a queue on said first access frequency by using a First-In-First-Out (FIFO) way; and

(2) outputting the image data in the horizontal direction in sequence on said first access frequency; and

(3) when running step(1) and step(2), both of them are working at the same access frequency.

5. The method for an image reducing processing circuit according to claim 4, wherein said first step First-In-First-Out (FIFO) unit has said memory depth is equal to a memory depth of said reduced image.

6. The method for an image reducing processing circuit according to claim 1, wherein providing said second step First-In-First-Out (FIFO) receiving said image data and transferring image data includes the following steps:

(1) reading said image data in said vertical direction, and writing said image data into said queue on the first access frequency by using said First-In-First-Out (FIFO) way; and

(2) outputting said image data in said vertical direction in sequence on said second access frequency; and

(3) when running step(1) and step(2), both of them are working at the deferent frequency.

7. The method for an image reducing processing circuit according to claim 6, wherein said second step First-In-First-Out (FIFO) unit has a one-input-one-output (FIFO) memory architecture implementing a transferring of the first and second access frequency.